School of Engineering and Natural Sciences / Electrical and Electronics Engineering (English)

2024 - 2025 Academic Year

EMBEDDED SYSTEMS

Syllabus

Course Description						
Name		**Code**	**Semester**	**T+A Hour**	**Credit**	**ECTS**
EMBEDDED SYSTEMS		EEE4210768	Spring Semester	3+2	4	8
Prerequisites Courses	MİKROİŞLEMCİLER					
Recommended Elective Courses						
Language of Instruction	English					
Course Level	First Cycle (Bachelor's Degree)					
Course Type	Elective					
Course Coordinator	Assist.Prof. Mustafa AKTAN					
Name of Lecturer(s)	Assist.Prof. Mustafa AKTAN					
Assistant(s)						
Aim	Mastering the hardware description language, Verilog HDL, for the design (specification, simulation, and synthesis) of digital systems and implementing them on FPGAs.					
Course Content	This course contains; Digital Systems Review,FPGA Systems,Digital System Modelling using Verilog,Verilog Modelling Styles: Structural,Verilog Modelling Styles: Dataflow,Verilog Modelling Styles: Behavioral,Design verification,Combinational circuit design using Verilog,Sequential circuit design using Verilog,Finite State Machine Design using Verilog,CPU Design,Synthesis,Implementation of Verilog design on FPGA,Design Optimization.					

Course Learning Outcomes	**Teaching Methods**	**Assessment Methods**
Structural, dataflow, and behavioral Modelling of digital blocks using Verilog HDL	10, 12, 14, 16, 17, 19, 2, 21, 5, 6, 9	A, E, F
Modelling, simulating, and testing combinational circuits in Verilog	10, 12, 14, 16, 17, 19, 2, 21, 5, 6, 9	A, E, F
Modelling, simulating, and testing sequential circuits in Verilog	10, 12, 14, 16, 17, 19, 2, 21, 5, 6, 9	A, E, F
Digital System Synthesis for FPGA	10, 12, 14, 16, 17, 19, 2, 21, 5, 6, 9	A, E, F
Digital System Optimization for FPGA	10, 12, 14, 16, 17, 19, 2, 21, 5, 6, 9	A, E, F

Teaching Methods	10: Discussion Method, 12: Problem Solving Method, 14: Self Study Method, 16: Question - Answer Technique, 17: Experimental Technique, 19: Brainstorming Technique, 2: Project Based Learning Model, 21: Simulation Technique, 5: Cooperative Learning, 6: Experiential Learning, 9: Lecture Method
Assessment Methods	A: Traditional Written Exam, E: Homework, F: Project Task

Lecture Schedule

Sequence	**Topics**	**Preliminary Preparation**
1	Digital Systems Review	Read the book
2	FPGA Systems	Read the book
3	Digital System Modelling using Verilog	Read the book
4	Verilog Modelling Styles: Structural	Read the book
5	Verilog Modelling Styles: Dataflow	Read the book
6	Verilog Modelling Styles: Behavioral	Read the book
7	Design verification	Read the book
8	Combinational circuit design using Verilog	Read the book
9	Sequential circuit design using Verilog	Read the book
10	Finite State Machine Design using Verilog	Read the book
11	CPU Design	Read the book
12	Synthesis	Read the book
13	Implementation of Verilog design on FPGA	Read the book
14	Design Optimization	Read the book

Evaluation Methods	**Weight(%)**
Midterm Exam	30
General Exam	70

Resources

Mano, Ciletti: Digital Design with an Introduction to the Verilog HDL, VHDL, and System Verilog, 6E

Thomas, Moorby: The Verilog Hardware Description Language